

Claims

What is claimed is:

- [c1] A circuit reduction method, comprising:
- inputting information about an original circuit structure;
 - using a resistive degree of at least one node in the original circuit structure to selectively sort the at least one node;
 - determining at least one time constant of the original circuit;
 - sorting the at least one time constant; and
 - determining whether to remove a loop in the original circuit structure based on the sorted at least one time constant and the sorted at least one node.
- [c2] The circuit reduction method of claim 1, further comprising preprocessing the original circuit structure.
- [c3] The circuit reduction method of claim 1, further comprising selectively choosing the at least one node as a node to be reduced.
- [c4] The circuit reduction method of claim 1, further comprising:
- determining another time constant of the original circuit after the loop has been removed from the original circuit structure;
 - sorting the another time constant; and
 - determining whether to remove another loop in the original circuit structure based on the sorted another time constant and the sorted at least one node.
- [c5] The circuit reduction method of claim 1, further comprising removing a loop that is not present in the original circuit structure but is present in an extraction of the original circuit structure.

- [c6] The circuit reduction method of claim 1, further comprising redistributing a resistance by eliminating another node that has an insignificant characteristic time constant depending on a local circuit transformation.
- [c7] The circuit reduction method of claim 1, further comprising redistributing a ground capacitance by eliminating another node that has an insignificant characteristic time constant depending on a local circuit transformation.
- [c8] The circuit reduction method of claim 1, further comprising maintaining an Elmore time constant from directions around the at least one node.
- [c9] A computer-readable medium having recorded therein instructions executable by processing, the instructions for:
- inputting information about an original circuit structure;
 - using a resistive degree of at least one node in the original circuit structure to selectively sort the at least one node;
 - determining at least one time constant of the original circuit;
 - sorting the at least one time constant; and
 - determining whether to remove a loop in the original circuit structure based on the sorted at least one time constant and the sorted at least one node.
- [c10] The computer-readable medium of claim 9, further comprising preprocessing the original circuit structure.
- [c11] The computer-readable medium of claim 9, further comprising selectively choosing the at least one node as a node to be reduced.
- [c12] The computer-readable medium of claim 9, further comprising:
- determining another time constant of the original circuit after the loop has been removed from the original circuit structure;

sorting the another time constant; and
determining whether to remove another loop in the original circuit structure
based on the sorted another time constant and the sorted at least one
node.

- [c13] The computer-readable medium of claim 9, further comprising removing a loop that is not present in the original circuit structure but is present in an extraction of the original circuit structure.
- [c14] The computer-readable medium of claim 9, further comprising redistributing a resistance by eliminating another node that has an insignificant characteristic time constant depending on a local circuit transformation.
- [c15] The computer-readable medium of claim 9, further comprising redistributing a ground capacitance by eliminating another node that has an insignificant characteristic time constant depending on a local circuit transformation.
- [c16] The computer-readable medium of claim 9, further comprising maintaining an Elmore time constant from directions around the at least one node.
- [c17] A computer system, comprising:
a processor;
a memory; and
instructions, residing in the memory and executable by the processor, for:
inputting information about an original circuit structure;
using a resistive degree of at least one node in the original circuit structure to selectively sort the at least one node;
determining at least one time constant of the original circuit;
sorting the at least one time constant; and
determining whether to remove a loop in the original circuit

structure based on the sorted at least one time constant and
the sorted at least one node.

- [c18] The computer system of claim 17, further comprising instructions for preprocessing the original circuit structure.
- [c19] The computer system of claim 17, further comprising instructions for selectively choosing the at least one node as a node to be reduced.
- [c20] The computer system of claim 17, further comprising instructions for:
determining another time constant of the original circuit after the loop has
been removed from the original circuit structure;
sorting the another time constant; and
determining whether to remove another loop in the original circuit structure
based on the sorted another time constant and the sorted at least one
node.
- [c21] The computer system of claim 17, further comprising instructions for removing a loop that is not present in the original circuit structure but is present in an extraction of the original circuit structure.
- [c22] The computer system of claim 17, further comprising redistributing a resistance by eliminating another node that has an insignificant characteristic time constant depending on a local circuit transformation.
- [c23] The computer system of claim 17, further comprising redistributing a ground capacitance by eliminating another node that has an insignificant characteristic time constant depending on a local circuit transformation.
- [c24] The computer system of claim 17, further comprising maintaining an Elmore time constant from directions around the at least one node.